Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A system for interconnecting two or more computer bus architectures, comprising:

a first bus segment to transmit data information;

a first half bridge circuit to connect said first bus segment;

a second bus segment to transmit data information;

a second half bridge circuit to connect said first half bridge circuit, said second half bridge circuit to transfer data information between said first bus segment and said second bus segment;

a plurality of data paths to connect said first half bridge circuit and said second half bridge circuit;

wherein said plurality of data paths to connect said first half bridge circuit and said second half bridge circuit are scalable to correspond to a bandwidth needed for a particular application.

2. (original) The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said first bus segment is a PCI architecture bus.

3. (original) The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said second bus segment is a PCI architecture bus.

4. (canceled)

5. (original) The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said first bus segment operates at a different bus frequency than a bus frequency of said second bus segment.

6. (original) The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said first bus segment operates at a substantially same bus frequency as a bus frequency of said second bus segment.

7. (original) The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

at least one of said first half bridge circuit and said second half bridge circuit are field programmable.

8. (original) The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said first half bridge circuit and said second half bridge circuit recover a clock signal from, respectively said first bus segment and said second bus segment.

9. (canceled)

10. (previously presented) A method of interconnecting two or more computer bus architectures comprising:

connecting a first half bridge circuit to a first bus segment;

connecting a second half bridge circuit to a second bus segment;

connecting said first bus segment to said second bus segment through a plurality of data paths connecting said first half bridge and said second half bridge; and

transmitting data information from said first bus segment to said second bus segment over at least one of said plurality of data paths;

wherein said plurality of data paths to connect said first half bridge circuit and said second half bridge circuit are scalable to correspond to a bandwidth needed for a particular application.

11. (previously presented) A method for interconnecting two or more computer bus architectures according to claim 10, wherein:

said step of transmitting data transmits data over a SCSI architecture bus.

12. (original) A method for interconnecting two or more computer bus architectures according to claim 10, wherein:

said step of transmitting data transmits data over a PCI architecture bus.

13. (canceled)

14. (original) A method for interconnecting two or more computer bus architectures according to claim 10, wherein:

operation of a bus frequency of said first bus segment is different than a bus frequency of said second bus segment.

15. (original) A method for interconnecting two or more computer bus architectures according to claim 10, wherein:

operation of a bus frequency of said first bus segment is substantially the same as a bus frequency of said second bus segment.

16. (original) A method for interconnecting two or more computer bus architectures according to claim 10, further comprising:

field programming at least one of said first half bridge circuit and said second half bridge circuit.

17. (original) A method for interconnecting two or more computer bus architectures according to claim 10, further comprising:

recovering a clock signal for said first half bridge circuit and said second half bridge circuit from their respectively connected said first bus segment and said second bus segment.

18. (canceled)

19. (previously presented) A system for interconnecting two or more computer bus architectures comprising:

a first half bridge circuit means connected to a first bus segment means;

a second half bridge circuit means connected to a second bus segment means; and

a plurality of data paths means to connect said first half bridge circuit means and said second half bridge circuit means;

wherein information is passed between said first bus segment means and said second bus segment means over said first half bridge circuit means and said second half bridge circuit means; and

wherein said said plurality of data paths means are scalable to correspond to a bandwidth needed for a particular application.

20. (original) The system for interconnecting two or more computer bus architectures according to claim 19, wherein:

said first bus segment is a PCI architecture bus.

21. (original) The system for interconnecting two or more computer bus architectures according to claim 19, wherein:

said second bus segment means is a PCI architecture bus.

22. (canceled)

23. (original) The system for interconnecting two or more computer bus architectures according to claim 19, wherein:

said first bus segment means bus frequency is different than said second bus segment means bus frequency.

24. (original) The system for interconnecting two or more computer bus architectures according to claim 19, wherein:

said first bus segment means bus frequency is the same as said second bus segment means bus frequency.

25. (original) The system for interconnecting two or more computer bus architectures according to claim 19, further comprising:

at least one of said first half bridge circuit means and said second half bridge circuit means are field programmable.

26. (previously presented) The system for interconnecting two or more computer bus architectures according to claim 19, further comprising:

said first half bridge circuit means and said second half bridge circuit means recover a clock signal from their respectively connected said first bus segment means and said second bus segment means.

27. (canceled)